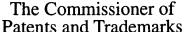
ARTIFACT SHEET

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The United States of America



Has received an application for a patent for a new and useful invention. The title and description of the invention are enclosed. The requirements of law have been complied with, and it has been determined that a patent on the invention shall be granted under the law.

Therefore, this

United States Patent

Grants to the person(s) having title to this patent the right to exclude others from making, using, offering for sale, or selling the invention throughout the United States of America or importing the invention into the United States of America for the term set forth below, subject to the payment of maintenance fees as provided by law.

If this application was filed prior to June 8, 1995, the term of this patent is the longer of seventeen years from the date of grant of this patent or twenty years from the earliest effective U.S. filing date of the application, subject to any statutory extension.

If this application was filed on or after June 8, 1995, the term of this patent is twenty years from the U.S. filing date, subject to any statutory extension. If the application contains a specific reference to an earlier filed application or applications under 35 U.S.C. 120, 121 or 365(c), the term of the patent is twenty years from the date on which the earliest application was filed, subject to any statutory extension.

I Toda I John

Acting Commissioner of Patents and Trademarks

allie M. Pusor



United States Patent [19]

Yano et al.

Patent Number: [11]

5,945,692

Date of Patent: [45]

*Aug. 31, 1999

[54] SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING SAME

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Assignee: Mitsubishi Denki Kabushiki Kaisha.

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This patent issued on a continued pros-[*] Notice: ecution application filed under 37 CFR

1.53(d). and is subject to the twenty year patent term provisions of 35 U.S.C.

154(a)(2).

[21] Appl. No.: 08/432,812

May 2, 1995 Filed: [22]

Foreign Application Priority Data [30]

[JP] Japan 6-118386 P [51] Int. Cl.⁶ H01L 29/74

[52] **U.S. Cl.** **257/139**; 257/212; 257/401; 257/630; 257/646; 257/649

Field of Search 257/139, 212. 257/341, 401, 630, 646, 649

References Cited [56]

U.S. PATENT DOCUMENTS

| 4 161 744 | 7/1070 | Blaske et al |
|-----------|---------|--------------|
| 4,101,744 | 111717 | 257/2 |
| 4 264 072 | 12/1082 | Becke et al |
| 4,304,013 | 12/1702 | 137/8 |
| 4.814.283 | 3/1989 | Temple et al |
| | | Ohtaka et al |
| 5,196,354 | 3/1993 | Ontaka et al |

5,521,409 5/1996 Hshieh et al. 257/341

FOREIGN PATENT DOCUMENTS

European Pat. Off. . 10/1983 0 091 079

10/1989 Japan . 1-265524 Japan . 2/1992 4-57330

5/1992 Japan . 4-130631

OTHER PUBLICATIONS

Patent Abstracts of Japan, vol. 14, No. 408 (E-972) (4351). Sep. 4, 1990, and JP 2 153570, Jun. 13, 1990.

IEEE Transactions on Electron Devices, vol. ED-27, No. 2, pp. 340-343, Feb. 1980. Richard W. Coen, et al., "A High-Performance Planar Power Mosfet".

Patent Abstracts of Japan, vol. 11, No. 275 (E-537) (2722). Sep. 5, 1987, and JP 62 73766, Apr. 4, 1987.

Patent Abstracts of Japan, vol. 16. No. 558 (E-1294), Nov. 27, 1992, and JP 4 212468, Aug. 4, 1992.

Primary Examiner-Sara Crane Attorney, Agent, or Firm-Oblon. Spivak. McClelland. Maier & Neustadt, P.C.

ABSTRACT

There is disclosed a semiconductor device having an MOS gate for reducing variations in threshold voltage (V_{th}) with time wherein a surface protective film is not formed in a device area including channels but only in a device peripheral area, thereby reducing the amount of hydrogen atoms migrating to a silicon-silicon oxide interface in a cell area and, accordingly, reducing the number of Si-H chemical bonds at the interface.

22 Claims, 11 Drawing Sheets

